ABSTRACT

According to one embodiment, a memory structure comprises a substrate having a channel region situated between a source region and a drain region. The memory structure further comprises a gate layer formed over the channel region of the substrate, and a tunable interlayer dielectric formed over the gate layer and the substrate. The tunable interlayer dielectric has a transparent state and an opaque state, and comprises a matrix and electrically or magnetically tunable material situated within the matrix. During the transparent state, UV rays can pass through the tunable interlayer dielectric to the gate layer, e.g., to perform a UV erase operation. During the opaque state, UV rays are prevented from passing through the tunable interlayer dielectric to the gate layer, thereby protecting the gate layer against unwanted charge storage and extrinsic damage that may occur during various processes.

Figure 1A should accompany the Abstract.